REMARKS

Claims 1-13, 17-21, and 23-25 are currently pending in the case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Section 103 Rejections

Claims 1-11, 17-19 and 23-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,862,242 to Wildi et al. (hereinafter "Wildi") in view of U.S. Patent No. 4,799,098 to Ikeda et al. (hereinafter "Ikeda"). In addition, claims 12, 13, 20, and 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wildi in view of U.S Patent No. 6,051,868 to Watanabe et al. (hereinafter "Watanabe"). To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974); MPEP 2143.03. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed.Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); and, MPEP 2143.01. The cited art does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

None of the cited art teaches or suggests, or can be combined or modified to teach or suggest, an integrated circuit with a buried layer of opposite conductivity than a well region formed above the buried layer, where the buried layer includes a first portion underlying a transistor formed within the well region and a second portion spaced apart from and laterally surrounding the first portion. Independent claim 1 recites in part:

> An integrated circuit, comprising ... a buried layer formed within a substrate below the well region, wherein the buried layer is of opposite conductivity type than the well region, and wherein the buried layer includes a first portion underlying the transistor and a second portion spaced apart from and laterally surrounding the first portion.

Support for such a limitation may be found, for example, in Fig. 8 in which circuit portion 40 includes a buried layer having first portion 86 and second portion 88 spaced by portion 90. As noted in the Office Action, "Wildi fails to disclose ... a buried layer include[ing] a first portion underlying the transistor and a second portion spaced apart from and laterally surrounding the first portion." (Office Action -- page 2). In

an attempt to overcome the deficiencies of Wildi, the Office Action cites Ikeda as disclosing "... a buried layer with various portions (2, 2', 14, 14') ..." and suggests "... it would have been obvious to one having ordinary skill in the art ... to modify the semiconductor device of Wildi to include a buried layer with various portions as disclosed in Ikeda because it aids in increasing the speed of the device ..." (Office Action -- page 2-3). The suggestion to combine the teachings of Ikeda and Wildi to teach the limitations of claim 1, however, are traversed as explained in more detail below.

As noted in a response to a previous Office Action mailed January 31, 2003, Ikeda does not teach or suggest a buried layer with a first portion and a second portion spaced apart and laterally surrounding the first portion. Although Ikeda teaches integrated circuits with buried layers 2, 2', 14 and 14', there is no teaching or suggestion within Ikeda that any of such buried layers are spaced apart from and laterally surround another of the buried layers. In other words, Ikeda fails to describe or illustrate any of buried layers 2, 2', 14 and 14' with an annular structure. Consequently, Ikeda fails to teach or suggest the limitations of claim 1. Since neither Ikeda nor Wildi teach or suggest a buried layer having an annular configuration, no combination of Ikeda or Wildi can teach or suggest the limitations of claim 1. To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974); MPEP 2143.03.

In addition to failing to teach a buried layer with a first portion and a second portion spaced apart and laterally surrounding the first portion, Ikeda fails to teach a buried layer formed below a well region of opposite conductivity as the buried layer. Rather, Ikeda specifically teaches, in reference to Figs. 2 and 7, p-type buried layer 14 formed underneath p-type well 5. Such a dual-layer same-conductivity region serves as a p-type well region for the NMOS transistor in Figs. 2 and 7 in which the thickness of epitaxial layers 3 and 3' is reduced (see, e.g., Ikeda, column 2, lines 6-13). Forming a buried layer of opposite conductivity below the well region, in such an embodiment, would drastically reduce the thickness of the well region and, consequently, increase the resistance of the well. As a result, electrical connection with a topside contact would be degraded. If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). MPEP 2143.01. Consequently, there is no motivation within Ikeda to provide an integrated circuit with a buried layer formed below a well region of opposite conductivity as the buried layer.

Furthermore, even if Ikeda taught or suggested a buried layer formed under a well region of opposite conductivity and/or with an annular structure, there is no motivation to combine Ikeda and Wildi to produce an integrated circuit with the limitations of claim 1. In particular, Wildi specifically teaches using a buried layer of opposite conductivity than the substrate and an overlying well region such that a device formed within the well region may be electrically isolated from the substrate. In contrast, Ikeda specifically discloses a buried layer with the same conductivity as an overlying well such that the electrical resistance of the well region may be decreased as described above. In particular, Ikeda teaches an NMOS transistor formed within p-type well 5 and having p-type buried layer 14 underneath. Such a configuration, however, does not electrically isolate the NMOS transistor from other devices within the circuit as necessitated by objective of Wildi. If the proposed modification or combination of the prior art would change the principle operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). MPEP 2143.01. As such, there is no motivation to combine the teachings of Wildi and Ikeda to create an integrated circuit with a buried layer of opposite conductivity type as the substrate and an overlying well region as recited in claim 1.

Furthermore, Watanabe cannot be combined with Wildi and/or Ikeda to overcome the deficiencies therein. Similar to Ikeda, Watanabe does not teach or suggest an integrated circuit with a buried layer of opposite conductivity type than an overlying well region. In addition, Watanabe does not provide any motivation to create an integrated circuit with such a limitation, since Watanabe specifically teaches that cross talk is undesirably generated by parasitic capacitance between layers of opposite conductivity type. Consequently, there is no motivation to combine Watanabe with Wildi and/or Ikeda to teach the limitations of claim 1.

None of the cited art teaches or suggests an integrated circuit having a doped annular region extending through a well region. Independent claim 17 recites in part: "[a]n integrated circuit, comprising ... a doped annular region extending through the well region to contact the buried layer..." Dependent claim 2 includes a similar limitation. As noted in a response to a previous Office Action mailed January 31, 2003, neither Wildi, Ikeda nor Watanabe teach or suggest having a doped annular region extending through a well region. In response to such an argument, however, the Examiner maintains that Wildi does disclose a doped annular region extending through a well region and supports such a contention by citing Fig. 3 in Wildi. Explicit reference of the doped annular region inferred in the Office Action is requested, since the inclusion of a doped annular region extending through well region 351 in Fig. 3 of

Wildi is not apparent to the Applicant. In particular, the only doped regions included within well region 351 are source region 352, drain region 354 and p+ region 364, none of which are annular or extend through well region 351. Although Wildi does teach high voltage region 316 surrounding transistor 350, high voltage region 316 does not extend through well region 351. Consequently, it is asserted that Wildi does not teach or suggest a device within a doped annular region extending through a well region as recited in claim 17. Furthermore, Ikeda and Watanabe fail to disclose a doped region extending through a well region, much less a doped annular region extending through a well region. Since none of the cited art teaches or suggests an integrated circuit with a doped annular region extending through a well region, no combination of the cited art can teach or suggest an integrated circuit with such a limitation. Consequently, claim 17 is asserted to be patentably distinct over the cited art.

For at least the reasons set forth above, none of the cited art, either individually or in combination, teaches, suggests, or provides motivation for all limitations of independent claims 1 and 17. Therefore, claims 1 and 17, as well as claims dependent therefrom, are patentably distinct over the cited art. Accordingly, Applicants respectfully request removal of this rejection.

In addition to being patentable for reasons set forth above, several of the dependent claims are believed to be separately patentable for reasons set forth below.

For example, claims 4 and 5 specify the distance between the first and second portions of the buried layer as recited in claim 1 as being less than about 5 microns and approximately 1.2 microns, respectively. The Office Action admittedly states that Wildi fails to disclose the limitations of claims 4 and 5. The Office Action further states that "... the applicant has not established the critical nature of the dimension of less than 5 microns..." and "... approximately 1.2 microns." Such statements are traversed, however, since the Specification clearly teaches the criticality of fabricating buried layer portions with such small separation distances to promote "pinching off" the lower end of the buried layer. In particular, the Specification states:

> The spacing needed between two such openings in the masking layer depends on the final separation of the buried layer portions desired, allowing for diffusion during processing. The final desired separation in turn depends on details, such as doping levels, of the particular fabrication process used. In some embodiments, for example, a masking layer spacing of about 2.1 microns may result in a post-processing separation of about 1.2 microns between the buried layer portions. In an embodiment, the separation between the buried layer portions after processing is such that the oppositely-doped region between the portions is "pinched off" during operation by depletion regions at the lower end of the

> buried layer, while retaining some undepleted material at the upper end of the buried layer. Such an embodiment is illustrated using dashed-line depletion region boundaries 90 in Fig. 8. The buried layer may separation be designed so that the "pinch-off" occurs when outer buried layer portion 88 is connected to VCC (for an n+ buried layer). This "pinch-off" may reduce substantially the coupling of noise generated by n-channel transistor 63 to p-type substrate 46. (Specification – page 15, lines 16-29)

As such, it is asserted that the Applicant has established the critical nature of the dimensions specified in claims 4 and 5.

With regard to claim 8, the cited art fails to provide an annular contact diffusion arranged laterally within the doped annular region and laterally surrounding the transistor. The Office Action, however, cites Wildi teaching such an annular contact diffusion in Fig. 3. As noted above in the argument regarding the patentability of independent claim 17, none of the cited art teaches or suggests an integrated circuit with a doped annular region within a well region, much less extending through a well region. As such, it is asserted that Wildi as well as Ikeda and Watanabe fail to teach or suggest an integrated circuit within an annular contact diffusion arranged laterally within a doped annular region of the circuit. Accordingly, claim 8 is asserted to be patentably distinct over the cited art.

In addition, the cited art fails to even teach or suggest the inclusion of a depletion region between the first and second portions of the buried layer as recited in claims 23-25. The Office Action cites Wildi teaching such a depletion region in Fig. 3. However, as noted above and in the Office Action, Wildi fails to teach a buried layer with a first portion and a second portion spaced apart from and laterally surrounding the first portion. Consequently, it is asserted that Wildi cannot teach the inclusion of a depletion region between separated portions of a buried layer as recited in claims 23-25. Accordingly, claims 23-25 are asserted to be patentably distinct over the cited art.

CONCLUSION

This response constitutes a complete response to all issues raised in the final Office Action mailed July 23, 2003. In view of the remarks traversing rejections, Applicants assert that pending claims 1-13, 17-21, and 23-25 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Conley Rose, P.C. Deposit Account No. 03-2769/5298-04500.

Respectfully submitted,

Mollie E. Lettang

Mollie E. Lettang
Reg. No. 48,405
Agent for Applicants

Conley Rose, P.C.
P.O. Box 684908
Austin, TX 78768-4908
Ph: (512) 476-1400
Date: September 23, 2003
MEL